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UNITED STATES PATENT APPLICATION

DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

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DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Field of the Invention

The present invention relates generally to electronic circuits. More particularly, it pertains to sense amplifiers operating with low voltage supplies.

Background of the Invention

Lower and lower power supply voltages are being employed on DRAM memory chips, which places more stringent requirements on the design parameters of sense amplifiers. It is difficult to get a conventional sense amplifier to have adequate response characteristics at these lower power supply voltages. Figure 1A is a schematic diagram illustrating a conventional cross-coupled sense amplifier. Figure 1B is a graph illustrating the very slow response of the conventional cross-coupled sense amplifier at a power supply voltage of 0.5V. As shown in Figure 1B, it can take up to nearly 100 nanoseconds (t = 100 ns) to achieve a significant sense signal and output voltage from the sense amplifier. This is far too long to be of any use in a conventional memory system.

Recently, synchronous body bias has been utilized in the sense amplifier designs in SOI technology with 0.9V power supply voltages on DRAMs. Examples of this are provided by: S. Kuge et al, "SOI-DRAM circuit technologies for low power high speed multigigascale memories," IEEE J. Solid-State Circuits, Vol. 31, pp. 586-591, April 1996; and K. Suma et al., "An SOI-DRAM with wide operating voltage range by CMOS/SIMOX technology," IEEE J. Solid-State Circuits, Vol 29, pp. 1323-1329, Nov. 1994. In the synchronous body bias arrangement, the body of the n-channel metal oxide semiconductor (NMOS) transistors are separately forward biased when the sense amplifier is activated to lower the magnitudes of the threshold voltages (Vt). This was found to be necessary to achieve reasonable response time from the sense amplifier at low power supply voltages. Unfortunately, the synchronous body bias arrangement requires extra clock or phase voltages, extra control lines and extra body contacts for the devices. These requirements quickly consume valuable surface area on the semiconductor chip.

Another technique to achieve improved performance from sense amplifiers includes the use of current sense amplifiers in the place of voltage sense amplifiers. Still another technique includes using gate-body connected transistors in the construction of the sense amplifier. Current sense amplifiers achieve a significant improvement in response by virtue of the fact that the voltage swing on the bit lines is very small, and by virtue of the fact that the large bit line capacitances are not connected to the output nodes. However, a current sense amplifier is not compatible with low power supply voltages. This is because the current sense amplifier is basically three devices are stacked up one atop another.

In its basic form, the three devices of a current differential amplifier include a current sink device, designed to provide common mode feedback and rejection, a pair of transistors for amplification, and a pair of load devices. Operation criteria demand that some significant overdrive, e.g., the excess in a transistor's gate to source potential (VGS) over the transistor's threshold voltage (VT), or (VGS-VT), is required in order to provide reasonable gain (G).

Another prior art method is basically to use a traditional sense amplifier and after firing the word line, dumping the charge onto the digitlines, then turn off the isolation transistors, perform the sensing process, and then once again turn the isolation transistors back on. This is one approach to attain high-speed sensing by separating the bitline capacitances at the expense of somewhat delaying your write back. However, there is still a delay between turning off the isolation transistors and firing the sense amplifier. And, still even better low-voltage designs are needed.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, it is desirable to develop sense amplifiers with improved response characteristics which can be fabricated according to a CMOS process and which can operate at power supply voltages of 1.0 V and below.

Summary of the Invention

The above- mentioned problems with sense amplifier configuration and operation as well as other problems are addressed by the present invention and will be understood by reading and studying the following specification. Structures and methods are provided which accord exemplary performance.

The new modified sense amplifier for low-voltage DRAMs is as much as 100 times faster than a conventional voltage sense amplifier when low power supply voltages, e.g. Vdd less than 1.0 Volts, are utilized. In the novel sense amplifier, the bit line capacitances are separated from the output nodes of the sense amplifier. High performance, wide bandwidth or very fast CMOS amplifiers are possible using the new circuit topology of the present invention.

A first embodiment includes a sense amplifier having a pair of cross-coupled invertors. Each inverter includes a transistor of a first conductivity type and a pair of transistors of a second conductivity type which are coupled at a drain region and are coupled at a source region. The drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type. A pair of input transmission lines are included where each one of the pair of input transmission lines is coupled to a gate of a first one of the pair of transistors in each inverter. A pair of output transmission lines are included where each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each invertor.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1A is a schematic diagram illustrating an embodiment of a convention sense amplifier.

Figure 1B is a graphical representation of the output voltage versus time (V-t) curve for the conventional sense amplifier shown in Figure 1A.

Figure 1C is a schematic diagram of a small signal equivalent circuit model for Figure 1A.

Figure 2A is a schematic illustration of a novel sense amplifier according to the teachings of the present invention.

Figure 2B is an V-t graph illustrating one embodiment of the operation of the novel sense amplifier circuit shown in Figure 2A.

Figure 2C is a schematic diagram of a small signal equivalent circuit model for Figure 2A.

Figure 3 illustrates one possible configuration for the inclusion of other transistors in the novel sense amplifier of Figure 2A as in normally done to achieve enable functions, and precharge and balance of the sense amplifier.

Figure 4 illustrates a memory circuit formed according to the teachings of the present invention.

Figure 5 is a block diagram illustrating an electronic system 500 according to the teachings of the present invention.

Detailed Description

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which are shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Figure 1A shows the schematic illustration of a conventional sense amplifier 100. The conventional sense amplifier 100 includes a pair of cross-coupled inverters, A1 and A2. Each inverter A1 and A2 includes a first transistor of a first conductivity type, T1 and T2, and includes a second transistor of a second conductivity type, T3 and T4. The transistors of the first and second conductivity type are coupled to one another at a drain region for each inverter, A1 and A2. A power supply voltage is coupled to node 6, and a ground potential is coupled to node 7 of the conventional sense amplifier 100. A pair of bit lines, BL1 and BL2, independently couple to the drain region for each inverter, A1 and A2. In the conventional sense amplifier 100 these drain regions additionally serve as the output nodes, V1 and V2, for the conventional sense amplifier 100. Thus, in the conventional sense amplifier 100 of Figure 1A the bit line, BL1 and BL2, capacitances are coupled to the output nodes, V1 and V2.

Figure 1B is a graphical representation of an output voltage versus time (V-t) curve for the conventional sense amplifier shown in Figure 1A. Figure 1B illustrates the responsiveness of the conventional sense amplifier operated with a

power supply of 0.5 Volts and where the transistors in the sense amplifier are constructed to have a threshold voltage V(t) of approximately 0.3 Volts. As shown in Figure 1B, the conventional sense amplifier has a relatively slow response time of 100 nanoseconds (t = 100 ns) when operating at this low power supply voltage (e.g. Vdd = 0.5 Volts).

Figure 1C is a schematic diagram of a small signal equivalent circuit model 101 of the conventional sense amplifier in Figure 1A. Again, the threshold voltage (Vt) magnitudes are fixed at about 0.3-0.35V for both the n-channel (NMOS) and p-channel (PMOS) transistors which make up the inverters of the cross-coupled inverters A1 and A2 of the conventional sense amplifier 100. During most of the switching transients the transistors are operating in the sub-threshold or threshold region since the power supple voltage is only Vdd = 0.5V. The sense amplifier output nodes and bit lines, BL1 and BL2, are initially balanced at Vdd/2 as is common in conventional voltage sense amplifiers. A disturbance is applied by discharging a memory cell 110 onto one of the bit lines, e.g. BL1. In this case a signal of 50 milliVolts (mV) is applied to one side of the sense amplifier. Due to the positive feedback in the cross-coupled configuration of inverters, the signal regenerates and a characteristic shape is obtained for the complementary output voltages which diverge as shown in Figure 1B.

An analysis of the operation of the conventional sense amplifier 100 in Figure 1A is provided in connection with reference to the small signal equivalent circuit model 101 of Figure 1C. The analysis shows that the magnitude of a voltage, VX, at node V2 in the conventional sense amplifier 100 increases linearly with time and that the magnitude of a voltage, VY, at node V1 of the conventional sense amplifier 100 increases quadratically with time. Here VY is equivalent to Vout on the conventional current sense amplifier 100.

As shown in Figure 1C, a voltage signal, ΔV, is placed onto the first bit line BL1 from a discharged memory cell on to bit line capacitance 110. For simplicity, and by way of illustration, the transistors have been assumed to be described by similar parameters and in particular similar transconductance parameters in the

device models. In practice, of course, the device sizes are ratioed and the PMOS transistors fabricated with a larger width to length (W/L) ratio. All transistors in the circuit, e.g., n-type and p-type, then have the same transconductance (where gm = gmn + gnp, and gmn = gmp) and drain conductance (where gd = gdn + gdp, and gdn = gdp). In operation, due to the voltage signal, ΔV, being coupled to node V1, the potential at node V1 increases. As node V1 of the first inverter raises to a high potential the cross-coupled nature of the inverters, A1 and A2, places the high potential on the gate of the p-channel transistor T4. Transistor T4 turns "off" and a voltage signal, VX, seen at node V2 on Figure 1, goes toward ground. At this point, a current signal, I2, is flowing at node V2 into a current source, which is transistor T2, and pulls bit line BL2 and node V2 toward ground. The current signal I2 can be expressed as $I2 = gm \times \Delta V$. I2 can also be expressed as $I2 = \Delta Q/t = CBL \times VX/t$. Substituting equivalent expression for I2 produces $gm \times \Delta V = CBL \times (VX)/t$. Solving for VX yields $VX = gm \times (\Delta V) \times t/CBL$.

The cross-coupled nature of the inverters, A1 and A2, provides feedback to the gates of transistors T1 and T3 in the first inverter A1. The feedback includes the voltage potential, VX, from node V2. This feedback turns "on" transistor T3. Turning "on" transistor T3 increases the conduction through transistor T3. At this point a voltage potential, VY, is present at node V1 and a current signal, I1, is exiting node V1 to bitline BL1. Here, the current signal I1 is expressed as $I1 = gm \times VX$. Similar to the above analysis, the current signal, I1, can also be expressed as $I1 = \Delta Q/\Delta t = CBL \times (VY)/t$. Substituting equivalent expressions for I1 produces $gm \times VX = CBL \times (VY)/t$.

Substituting the value of VX from above, i.e. $VX = gm \times \Delta V \times t/CBL$, yields $gm \times (gm \times \Delta V \times t)/CBL = CBL \times (VY)/t$.

Solving for VY where VY is equivalent to Vout yields,

$$VOUT^{+} = VY = (gm/CBL)^{2} \times \Delta V \times t^{2} \quad \text{.....(1)}$$

As stated above, gm is the effective transconductance of the n-channel and p-channel transistors or the sum of the individual transconductances, CBL is the bit-line capacitance, ΔV is the initial signal injected into the conventional sense amplifier from the bit line, BL1, and t is the signal rise time.

As is illustrated in detail in Figure 1C, the output voltage increases relatively slowly as the square of time. The problem with a conventional voltage sense amplifier is that the bit line capacitance CBL is so large, e.g., can be up to 200 femto Farads (fF) in magnitude, that the output sense signal, Vout, is delayed. That is, the transconductance of transistors in the conventional sense amplifier, when operated with low voltages, is relatively small. This results in an insufficient response time for the conventional sense amplifier 100.

In one example, the full transconductance of both full-size transistors constituting each inverter, A1 and A2, is gm = 20 microsiemens (μS). The bit line, BL1 and BL2, capacitances are approximated at 200 fF. Solving for t from the equation (1) gives $t = CBL/gm \sqrt{Vout / \Delta V}$. That is, $t \approx 10 \text{ ns} \sqrt{Vout / \Delta V}$.

Figure 2A is a schematic diagram illustrating a novel sense amplifier circuit 200, latch circuit 200, or amplifier circuit 200 according to the teachings of the present invention. The novel sense amplifier circuit 200 includes a voltage sense amplifier where the bit lines, BL1 and BL2 are removed from the output nodes V1 and V2. This results in much faster response time. And in the novel sense amplifier circuit 200 only two devices, the minimal number, are stacked up. Figure 2A shows only the basic circuit without the extra transistors as normally required for enable and balancing functions.

As shown in Figure 2A, the sense amplifier 200 includes a pair of cross-coupled inverters, B1 and B2, or cross-coupled amplifiers, B1 and B2. Each inverter, B1 and B2, includes a first transistor of a first conductivity type, M1 and M2 respectively. In one embodiment, the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor. As shown in Figure 2A, the NMOS transistors T1 and T2 in the conventional sense amplifier 100 of Figure 1A are each divided into two separate transistors. Thus, each inverter, B1

and B2, includes a second transistor, M3 and M4 respectively, and includes a third transistor, M5 and M6 respectively, each of a second conductivity type.

The second transistor, M3 and M4, and third transistor, M5 and M6, in each inverter, B1 and B2, are coupled at a drain region, 204 and 206 respectively. The second transistor, M3 and M4, and third transistor, M5 and M6, in each inverter, B1 and B2, are also coupled at a source region, 208 and 210 respectively. In this manner, the second transistor, M3 and M4, and the third transistor, M5 and M6, in each inverter, B1 and B2, form a pair of transistors, M3, M5, and M4, M6 respectively, of a second conductivity type in each inverter, B1 and B2. In one embodiment, the pair of transistors, M3, M5, and M4, M6 respectively, includes a pair of n-channel metal oxide semiconductor (NMOS) transistors. Further, the drain region, 204 and 206, in each pair of transistors, M3, M5, and M4, M6, is coupled to a drain region, 212 and 214 respectively, of the transistor of the first conductivity type, M1 and M2.

A pair of input transmission lines, bit lines, or digitlines, 221 and 222, couple to the sense amplifier 200. Each one of the pair of input transmission lines, 221 and 222, is coupled to a gate of one of the transistors in the pair of transistors, M3, M5, and M4, M6 inverter. In the embodiment shown in Figure 2A, each one of the pair of input transmission lines, 221 and 222, is coupled to a gate, 223 and 225 respectively, of a first one, or first transistor, M3 and M4, in the pair of transistors, M3, M5, and M4, M6, in each inverter, B1 and B2. As shown in Figure 2A, the bit line, 221 and 222, capacitances are removed from the pair of output transmission lines

The first inverter B1 and the second inverter B2 are cross-coupled. As shown in Figure 2A, the drain region 204 of the pair of transistors M3, M5 and the drain region 212 of the transistor of the first conductivity type M1 in inverter B1 is further coupled to a gate 251 of the transistor of a first conductivity type M2 and to a gate 253 of a second one, or second transistor, M6, of the pair of transistors, M4, M6, in the other inverter, B2. Similarly, the drain region 206 of the pair of transistors M4, M6 and the drain region 214 of the transistor of the first conductivity

type, M2, in inverter B2 is further coupled to a gate 252 of the transistor of a first conductivity type, M1, and to a gate 254 of a second one, or second transistor, M5, of the pair of transistors, M3, M5, in the other inverter, B2.

A pair of output transmission lines, 230 and 232, are coupled to the sense amplifier 200. Each one of the pair of output transmission lines is coupled to the drain region, 204 and 206, of the pair of transistors, M3, M5, and M4, M6 and the drain region, 212 and 214 of the transistor of the first conductivity type, M1 and M2, in each inverter, B1 and B2. In the novel sense amplifier 200 shown in Figure 2A a source region, 261 and 262, for the first transistor, or transistor of first conductivity type, M1 and M2 respectively in each inverter, B1 and B2 is coupled to a power supply voltage at node 6. In one embodiment, the power supply voltage at node 6 is less than 1.0 Volts. The novel sense amplifier 200 also has a ground node, RNL or node 7. In one embodiment, the RNL or node 7 is coupled to ground. In an alternative embodiment, the RNL or node 7 is coupled is coupled to a different voltage potential, e.g. a voltage potential lower than ground.

In an alternative embodiment, the pair of transistors, M3, M5, and M4, M6, in each inverter, B1 and B2, comprise a dual-gated metal oxide semiconductor field effect transistor (MOSFET) in each inverter, B1 and B2. In this embodiment, each one of the pair of input transmission lines is coupled to a first gate of the dual-gated MOSFET in each inverter, B1 and B2. In this embodiment, the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and the a dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors, each driven by one of the dual gates. In this embodiment, the drain regions, 204 and 212, for one of the cross-coupled inverters, B1, is further coupled to a gate of the transistor of the first conductivity type, M2, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2. Similarly, the drain regions, 206 and 214, for inverter, B2, is coupled to a gate of the transistor of the first conductivity type, M1, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2.

Figure 2B is a graphical representation of an output voltage versus time (V-t) curve for the novel sense amplifier shown in Figure 2A. Again, in the modified new sense amplifier configuration of Figure 2A the bit line capacitance is not connected to the output nodes, V1 and V2. In Figure 2A, each n-channel transistor, T1 and T2, of Figure 1A is divided in half into two separate transistors, and each bit line, BL1 and BL2, is connected separately to one of these additional transistors. Figure 2B illustrates the responsiveness of the novel sense amplifier operated with a power supply of 0.5 Volts and where the transistors in the sense amplifier are constructed to have a threshold voltage of approximately 0.3 Volts. As shown in Figure 2B, the novel sense amplifier of the present invention has much faster response time of less than 10 nanoseconds (t = 10 ns).

Figure 2C is a schematic diagram of a small signal equivalent circuit model of the novel sense amplifier 200, shown in Figure 2A. Again, the threshold voltage (Vt) magnitudes are fixed at about 0.3-0.35V for both the n-channel (NMOS) and p-channel (PMOS) transistors which make up the inverters of the cross-coupled inverters, B1 and B2, of the novel sense amplifier 200. During most of the switching transients the transistors are operating in the sub-threshold or threshold region since the power supple voltage is only Vdd = 0.5V. The sense amplifier output nodes and bit lines are initially balanced at Vdd/2 as is common in conventional voltage sense amplifiers. A disturbance is applied by discharging a memory cell onto the capacitance 210 of the bit lines, e.g. BL1. In this case a signal of 50 milliVolts (mV) is applied to one side of the sense amplifier. Due to the positive feedback in this cross-coupled configuration of inverters, the signal regenerates and a characteristic shape is obtained for the complementary output voltages which diverge as shown in Figure 2B.

An analysis of the operation of the novel sense amplifier 200 in Figure 2A is provided in connection with reference to the small signal equivalent circuit model 201 of Figure 2C. Here VY is equivalent to Vout on the novel current sense amplifier 200. As shown in Figure 2C, a voltage signal, ΔV, placed onto the capacitance 210 of the first bit line BL1 from a discharged memory cell drives the

gate 223 of transistor M3 on the left hand side, or first side, of the novel sense amplifier 200. Driving the gate of this NMOS transistor increases the conduction flowing through transistor M3. This results in a decreasing voltage potential, VZ, at node V1.

At this point, a current signal, I2, associated with the voltage potential, VZ, is flowing at node V1. Since the voltage signal, ΔV, only drives the gate 223 of transistor M3, the transconductance, gm, at node V1 is only one-fourth the value seen at node V1 in Figure 1A. I2 can be expressed as $I2 = gm \times \Delta V/4$. I2 can also be expressed as $I2 = \Delta Q/t = CS \times VZ/t$, where CS is the stray capacitance value. Substituting equivalent expressions for I2 produces $gm \times \Delta V/4 = CS \times (VZ)/t$. Solving for VZ yields $VZ = (1/4) \times (gm/CS) \times (\Delta V) \times t$.

The voltage potential, VZ, at node V1 is coupled to a gate 251 of the PMOS transistor, M2, and to a gate 253 of NMOS transistor M6. The decreasing voltage potential, VZ, at node V1 places a lower potential on the gate of PMOS transistor, M2. As a result, transistor M2 turns "on" and transistor M6 turns "off." Here, the NMOS transistor, T2, on the right hand side, or second side, of the conventional sense amplifier 100 of Figure 1A has been replace by two NMOS transistors, M4 and M6 in the novel sense amplifier 200 of Figure 2A. Since VZ only drives the gates, 251 and 253, of M2 and M6, the transconductance, gm, at node V2 is three-fourths the value seen at node V2 in Figure 1A, e.g. a slightly lower transconductance.

At this point, a voltage potential, VX, is present at node V2 and a current signal, I3, is flowing at node V2. I3 can be expressed as $I3 = (3/4) \times gm \times VZ$. The current signal I3 can also be expressed as $I3 = \Delta Q/t = CS \times VX/t$, where CS is the stray capacitance value. Substituting equivalent expressions for I3 produces $(3/4) \times gm \times VZ = CS(VX)/t$. Substituting the value of VZ from above, i.e. $VZ = (1/4) \times (gm/CS) \times (\Delta V) \times t$, into the equation yields $(3/4) \times gm \times (1/4) \times (gm/CS) \times (\Delta V) \times t = CS \times (VX)/t$. Solving for VX then yields $VX = (3/16) \times (gm/CS)^2 \times (\Delta V) \times t^2$.

The cross-coupled nature of the inverters, B1 and B2, provides a feedback to the gates of transistors M1 and M5 in the first inverter B1. The feedback includes

the voltage potential, VX, from node V2. This feedback turns "off" transistor M1 and turns "on" transistor M5. Turning "off" transistor M1 decreases the conduction through transistor M1. Turning "on" transistor M5 increases the conduction through transistor M5. As explained above, the NMOS transistor, T1, on the left hand side, or second side, of the conventional sense amplifier 100 of Figure 1A has been replace by two NMOS transistors, M3 and M5 in the novel sense amplifier 200 of Figure 2A. Since VX only drives the gates, 252 and 254, of M1 and M5, the transconductance, gm, at node V1 is three-fourths the value seen at node V1 in Figure 1A, i.e., a slightly lower transconductance.

At this point, a voltage potential, VY, is present at node V1. The decreased conduction through transistor M1, and increased conduction through transistor M5, provides a current signal, I1, flowing at node V1. Here again, similar to the above analysis $I1 = (3/4)\times gm\times VX$. The current signal I1 can also be expressed as $I1 = \Delta Q/t = CS\times(VY)/t$. Substituting equivalent expressions for I1 produces $(3/4)\times gm\times VX = CS\times(VY)/t$. Substituting into this equation the value of VX from above, i.e. $VX = (3/16)\times(gm/CS)^2\times(\Delta V)\times t^2$, yields

$$(3/4)\times gm\times(3/16)\times(gm/CS)^2\times(\Delta V)\times t^2 = CS\times(VY)/t.$$

Solving for VY where VY is equivalent to Vout at node V1, yields

$$VOUT- = VY = (9/64)\times (gm/CS)^3\times\Delta V\times t^3 \quad \text{.....(2)}$$

Again, gm is the effective transconductance of the n-channel and p-channel transistors or the sum of the individual transconductances. CS represents the stray capacitances connected to the output nodes, the input capacitances of subsequent amplifiers connected to nodes V1 and V2. As shown in equation (2), the output has a slightly different power law dependence on time, now cubic. The novel sense amplifier has a slightly lower transconductance, gm, of the transistors in the cross-coupled inverters, B1 and B2, (e.g. cross-coupled latch, or latch circuit) which is approximately three-fourths of the original value of that in Figure 1A. However, a much faster response time is provided for obtaining a full output sense voltage since

the output nodes only need to drive the small stray capacitances of the nodes, V1 and V2, and the input capacitances of the subsequent amplifiers. There is also no delay associated with turning off the isolation transistors. According to the present invention, you can fire the sense amplifier as soon as the charge is placed on the digit lines, or bit lines. The net result is that the response might be as much as 100 times faster since CS might typically be more like a few femto Farads (fF), e.g. 2.5 fF, rather than 200 fF or so for the bit line capacitances as in the conventional sense amplifier of Figure 1A.

In one example, the full transconductance of both full-size transistors constituting each inverter, B1 and B2, is gm = 20 microsiemens (μS). The bit line, BL1 and BL2, capacitances are approximated at 200 fF. The stray capacitances, CS, are taken as 2.5 femto Farads (fF). Solving for t from the equation (2) gives $t = CS/gm \sqrt[3]{64/9\ Vout/\Delta V}$. That is, $t \approx 0.1$ ns $\sqrt[3]{64/9\ Vout/\Delta V}$.

Figure 3 shows the sense amp with extra transistors for enable and balance. Figure 3 illustrates one possible configuration for the inclusion of other transistors as in normally done to achieve enable functions, and precharge and balance of the sense amplifier. Transistors ME are used to select and enable the sense amplifier. Transistors MA, MB, and MC can be used to balance the amplifier and bit lines after the bit lines are precharged by other transistors at for instance the ends of the bit lines, not shown here. After balance is achieved, these transistors are turned off and the signal sensed by discharging a storage capacitance, Cstorage, from a memory cell coupled onto the capacitance 310 of one of the bit lines. At the completion of the sense cycle the original data can be written back into the cell by activating transistors MA and MB.

Figure 4 illustrates a memory circuit 400 formed according to the teachings of the present invention. The memory circuit 400 includes a number of memory cell arrays, shown in Figure 4 as ARRAY 0 and ARRAY 1. Each of the number of memory cell arrays, ARRAY 0, ARRAY 1, etc., a number of memory cells, MC1, MC2, . . ., MCn, arranged in row and columns. The number of memory cells, MC1, MC2, . . ., MCn, are coupled to wordlines. The memory circuit 400 includes at least

one sense amplifier 490 as described and presented in detail above in connection with Figure 2A. The at least one sense amplifier 490 has a power supply node, ACT or node 6. In one embodiment, the power supply node is coupled to a power supply voltage of less than 1.0 Volts. The at least one sense amplifier 490 also has a ground node, RNL or node 7. In one embodiment, the RNL or node 7 is coupled to ground. In an alternative embodiment, the RNL or node 7 is coupled is coupled to a different voltage potential, e.g. a voltage potential lower than ground.

The memory circuit includes a number of complementary pairs of bit lines or digitlines, shown in Figure 4 as D1, D1* and D2, D2*. The complementary pairs of bit lines, D1, D1* and D2, D2*, couple the at least one sense amplifier 490 to the number of memory cells, MC1, MC2, . . ., MCn, contained in the number of memory cell arrays, ARRAY 0, ARRAY 1, etc. The complementary pairs of bit lines, D1, D1* and D2, D2*, also couple to the at least one sense amplifier 490 in the manner presented and described in detail in connection with Figure 2A.

The memory circuit 400 includes a number of equilibration transistors, EQA, EQB, etc, and at least one enable transistor, ME, which couple to the complementary pairs of bit lines, D1, D1* and D2, D2*, and to the at least one sense amplifier 490 as shown in Figure 4. The memory circuit 400 includes a pair of output transmission lines, or input/output lines, shown in Figure 4 as I/O and I/O*. The output transmission lines, I/O and I/O*, are operatively coupled to output nodes, V1 and V2, on the at least one sense amplifier 490 through access transistors, AC1 and AC2 respectively. A column select line, shown in Figure 4 as CSEL, couples to the gates of the access transistors, AC1 and AC2.

The memory circuit 400 includes a number of isolation transistors, shown in Figure 4 as ISOA and ISOB. The number of isolation transistors, ISOA and ISOB, also couple to the complementary pairs of bit lines, D1, D1* and D2, D2*, and to the at least one sense amplifier 490 and can isolate the at least one sense amplifier 490 from the complementary pairs of bit lines, D1, D1* and D2, D2*. In one embodiment, the memory circuit 400 includes a folded bit line, or folded digitline memory circuit 400 as shown in Figure 4. In an alternative embodiment, the

memory circuit 400 includes other digitline configuration schemes as will be understood by one of ordinary skill in the art upon reading this disclosure.

Figure 5 is a block diagram illustrating an electronic system 500 according to the teachings of the present invention. The electronic system 500 includes a processor or processing unit 510 and a memory device 520, e.g. a random access memory (RAM). A bus 530 communicatively couples the processing unit 510 and the memory device 520. In one embodiment, the bus 530 includes a system bus, a serial connection, or other bus. In one embodiment, the processor unit 510 and the memory device 520 are on a single semiconductor wafer. In an alternative embodiment, the processor unit 510 and the memory device 520 are on two separate semiconductor wafers. The memory device 520 further includes a sense amplifier, latch circuit, amplifier circuit, or memory circuit, as described and presented in detail above in connection with Figures 2A, 3, and 4.

Conclusion

A structure and method for improving differential amplifier operation are provided. High performance, wide bandwidth or very fast CMOS amplifiers are possible using the new circuit topology of the present invention. The new modified sense amplifier for low voltage DRAMs is as much as 100 times faster than a conventional voltage sense amplifier when low power supply voltages, e.g. Vdd less than 1.0 Volts, are utilized. In the novel sense amplifier, the bit line capacitances are separated from the output nodes of the sense amplifier.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any

other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of a first one of the pair of transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

2. The sense amplifier of claim 1, wherein the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the pair of transistors of a second conductivity type are n-channel metal oxide semiconductor (NMOS) transistors.

3. The sense amplifier of claim 1, wherein the drain region for the pair of transistors and the drain region for the transistor of the first conductivity type in one inverter is further coupled to a gate of the transistor of a first conductivity type and to a gate of a second one of the pair of transistors in the other inverter.

4. A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor;

and

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;

a bit line coupled to each inverter, wherein each bit line couples to a gate for a first one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region for the PMOS and the NMOS transistors.

5. The sense amplifier of claim 4, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled inverters is further coupled to a gate of the PMOS transistor and to a gate of a second one of the pair of NMOS transistors in the other one of the cross-coupled inverters.

6. The sense amplifier of claim 4, wherein the bit line capacitances are removed from the pair of output transmission lines.

7. The sense amplifier of claim 6, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

8. The sense amplifier of claim 4, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

9. The sense amplifier of claim 8, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

10. A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a second transistor and a third transistor of a second conductivity type, wherein the second and third transistors are coupled at a drain region and are coupled at a source region, and wherein the drain region for the second and third transistors are coupled to a drain region of the first transistor;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a gate of the second transistor in each amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the second and the third transistors.

11. The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second and the third transistors include n-channel metal oxide semiconductor (NMOS) transistors.

12. The latch circuit of claim 11, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled amplifiers is further coupled to a gate of the PMOS transistor and to a gate of a third transistor in the other one of the cross-coupled amplifiers.

13. The latch circuit of claim 10, wherein the pair of input transmission lines are bit lines and wherein the bit line capacitances are removed from the pair of output transmission lines.

14. The latch circuit of claim 13, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

15. The latch circuit of claim 10, wherein the latch circuit is coupled to a power supply voltage of less than 1.0 Volts.

16. The latch circuit of claim 10, wherein the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns).

17. An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the first transistor of a first conductivity type and the a dual-gated MOSFET are coupled at a drain region;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a first gate of the dual-gated MOSFET; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

18. The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the a dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

19. The amplifier circuit of claim 17, wherein the drain region for one of the cross-coupled inverters is further coupled to a gate of the transistor of the first conductivity type and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters.

20. The amplifier circuit of claim 17, wherein the pair of cross-coupled inverters comprise a sense amplifier, and wherein the sense amplifier is included in a memory circuit.

21. The amplifier circuit of claim 20, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

22. The amplifier circuit of claim 21, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

23. A memory circuit, comprising:

a number of memory arrays;

at lease one sense amplifier, wherein the sense amplifier includes:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to a gate of a first one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the pair of NMOS transistors in each inverter.

24. The memory circuit of claim 23, wherein the memory circuit includes a folded bit line memory circuit.

25. The memory circuit of claim 23, wherein the drain region for the PMOS and the NMOS transistors in one of the cross-coupled inverters is further coupled to a

gate of the PMOS transistor and to a gate of a second one of the pair of NMOS transistors in the other one of the cross-coupled inverters.

26. The memory circuit of claim 23, wherein the at least one sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

27. The memory circuit of claim 23, wherein the at least one sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

28. The memory circuit of claim 23, wherein the memory circuit further includes a number of equilibration and a number of isolation transistors coupled to the complementary pair of bit lines.

29. An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a pair of n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor is coupled to the drain region for the pair of NMOS transistors;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to a

gate of a first one of the pair of NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the pair of NMOS transistors in each inverter.

30. The electronic system of claim 29, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volt.

31. The electronic system of claim 29, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

32. An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to a gate of a first one of the pair of transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

33. A method for forming a current sense amplifier, comprising:

cross coupling a pair of inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type; and

wherein cross coupling the pair of inverters includes coupling the drain region for the transistor of the first conductivity type and the drain region for the pair of transistors in one inverter to a gate of the transistor of a first conductivity type and to a gate of a first one of the pair of transistors in the other inverter.

34. The method of claim 33, wherein cross coupling the pair of inverters includes forming the first transistor of the first conductivity type as a p-channel metal oxide semiconductor (PMOS) transistor, and forming the pair of transistors of a second conductivity type as n-channel metal oxide semiconductor (NMOS) transistors.

35. The method of claim 33, wherein the method further includes coupling a bit line to a gate of a second one of the pair of transistors in each inverter.

36. The method of claim 33, wherein the method further includes coupling an output transmission line to the drain region for the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

37. A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a second transistor and a third transistor of a second conductivity type, wherein forming the second and the third transistors includes coupling a drain region and a source region for the second and third transistors, and coupling the drain region for the second and third transistors to a drain region of the first transistor;

coupling a bit line to a gate of the second transistor in each inverter; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the second and the third transistors in each inverter.

38. The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the second and third transistors of a second conductivity type includes forming n-channel metal oxide semiconductor (NMOS) transistors.

39. The method of claim 37, wherein cross coupling the pair of inverters includes coupling the drain region for second and third transistors and the drain region for the first transistor of the first conductivity type in one inverter to a gate of the first transistor of a first conductivity type and to a gate of a third transistor in the other inverter.

40. A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a gate of a first NMOS transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a gate of a first NMOS transistor in a second inverter in the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a second NMOS transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a gate of a second NMOS transistor in the first inverter.

41. The method of claim 40, wherein operating the sense amplifier includes operating the sense amplifier with a power supply voltage of less that 1.0 Volts.

42. The method of claim 40, wherein operating the sense amplifier includes latching an output sense signal in less than 10 nanoseconds (ns).

43. The method of claim 40, wherein the method further includes removing the bit line capacitance from a pair of output nodes of the sense amplifier.

44. A method for operating a sense amplifier, comprising:

providing a first bit line signal to a gate of a first NMOS transistor coupled at a drain region and a source region to a second NMOS transistor in a first inverter of the sense amplifier;

providing a second bit line signal to a gate of a first NMOS transistor coupled at a drain region and a source region to a second NMOS transistor in a second inverter of the sense amplifier; and

wherein providing the first and the second bit line signals to the gates of the first and second NMOS transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

45. A method for operating a sense amplifier, comprising:

providing an input signal from a bit line to a gate of a first transistor in a first inverter of the sense amplifier; and

wherein providing the input signal to the gate of the first transistor isolates the bit line capacitance from an output node on the sense amplifier.

DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Abstract of the Disclosure

Structures and methods for improving sense amplifier operation are provided. A first embodiment includes a sense amplifier having a pair of cross-coupled inverters. Each inverter includes a transistor of a first conductivity type and a pair of transistors of a second conductivity type which are coupled at a drain region and are coupled at a source region. The drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type. A pair of input transmission lines are included where each one of the pair of input transmission lines is coupled to a gate of a first one of the pair of transistors in each inverter. A pair of output transmission lines is included where each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

High performance, wide bandwidth or very fast CMOS amplifiers are possible using the new circuit topology of the present invention. The new modified sense amplifier for low voltage DRAMs is as much as 100 times faster than a conventional voltage sense amplifier when low power supply voltages, e.g. Vdd less than 1.0 Volts, are utilized. In the novel sense amplifier, the bit line capacitance is separated from the output nodes of the sense amplifier.

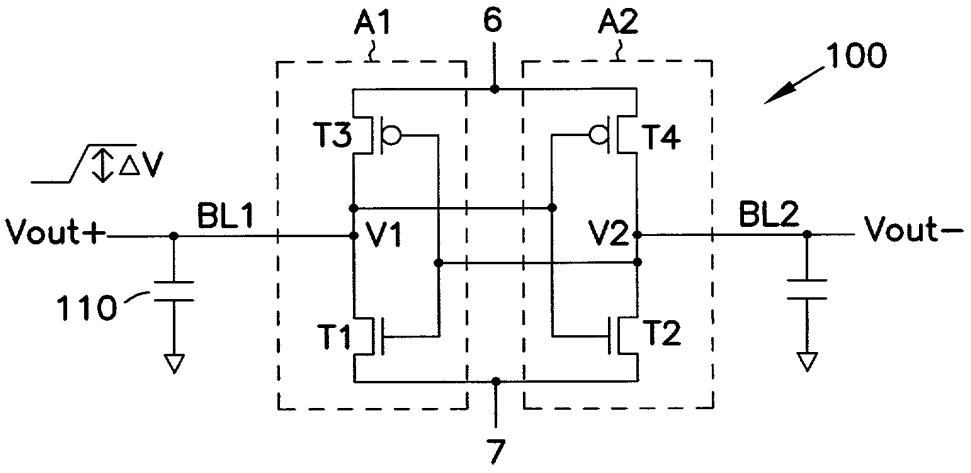


FIG. 1A (PRIOR ART)

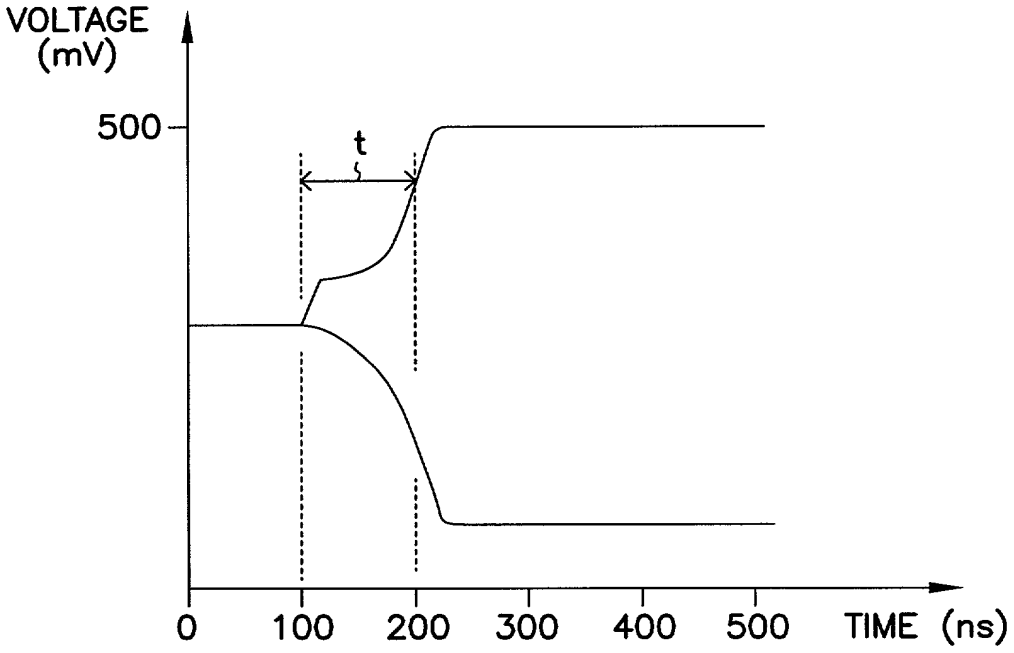


FIG. 1B (PRIOR ART)

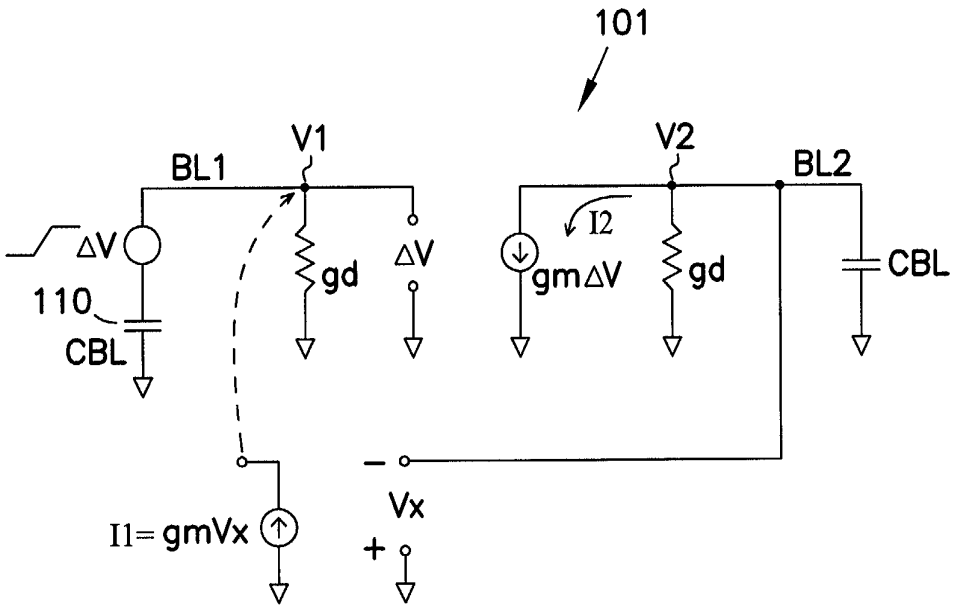
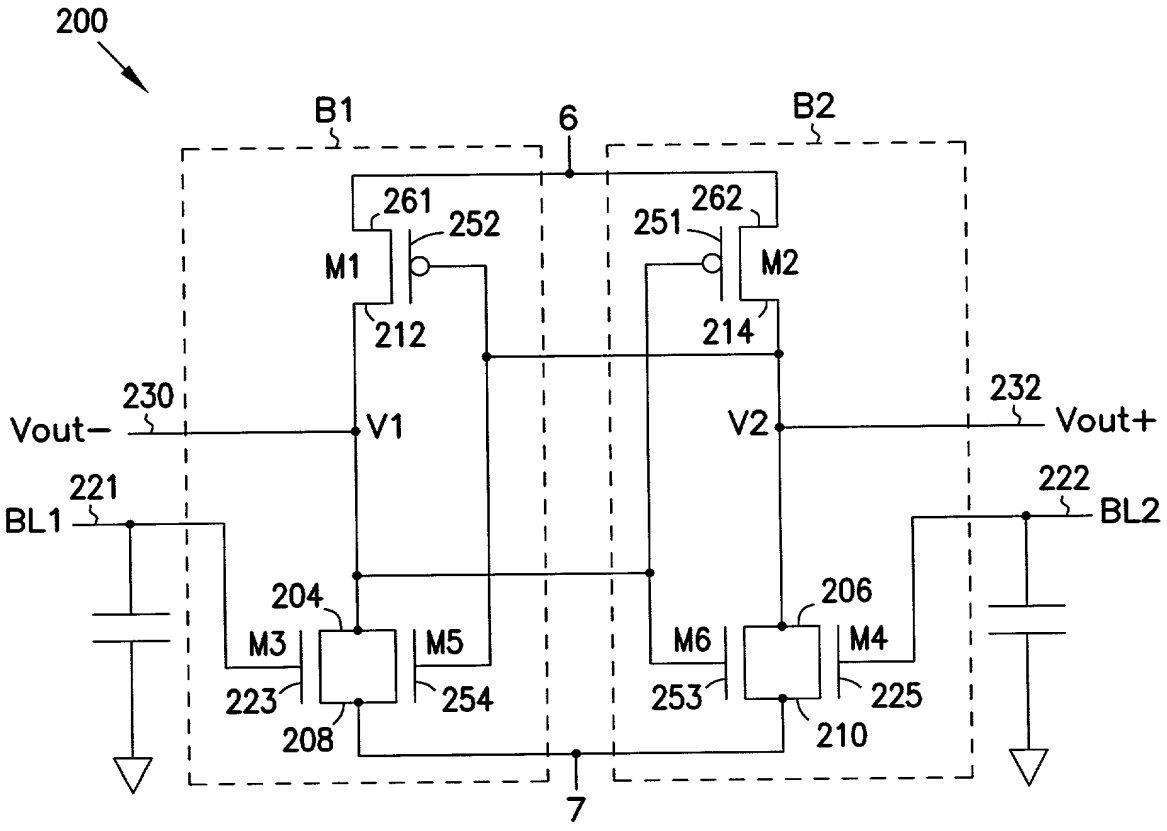


FIG. 1C


200
B1
6
B2
261
252
251
262
M1
M2
212
214
230
232
Vout−
V1
V2
Vout+
221
222
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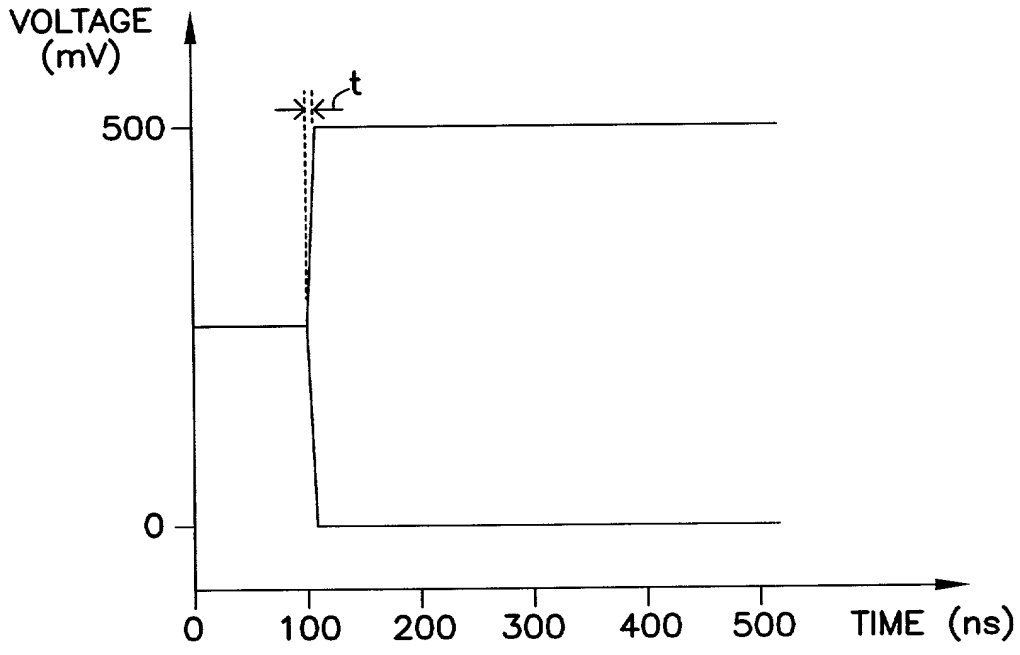
M3
M5
M6
M4
223
254
253
225
208
210
7

FIG. 2A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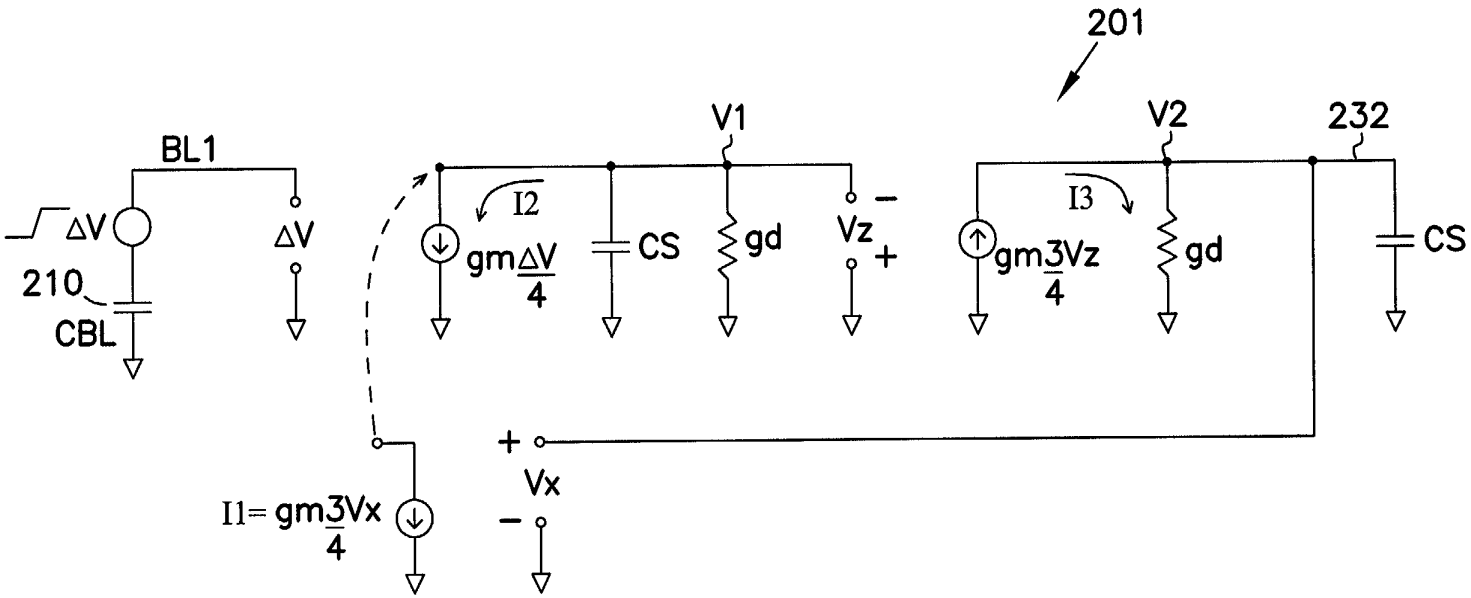
(mV)
t
500
0
0
100
200
300
400
500
TIME (ns)

FIG. 2B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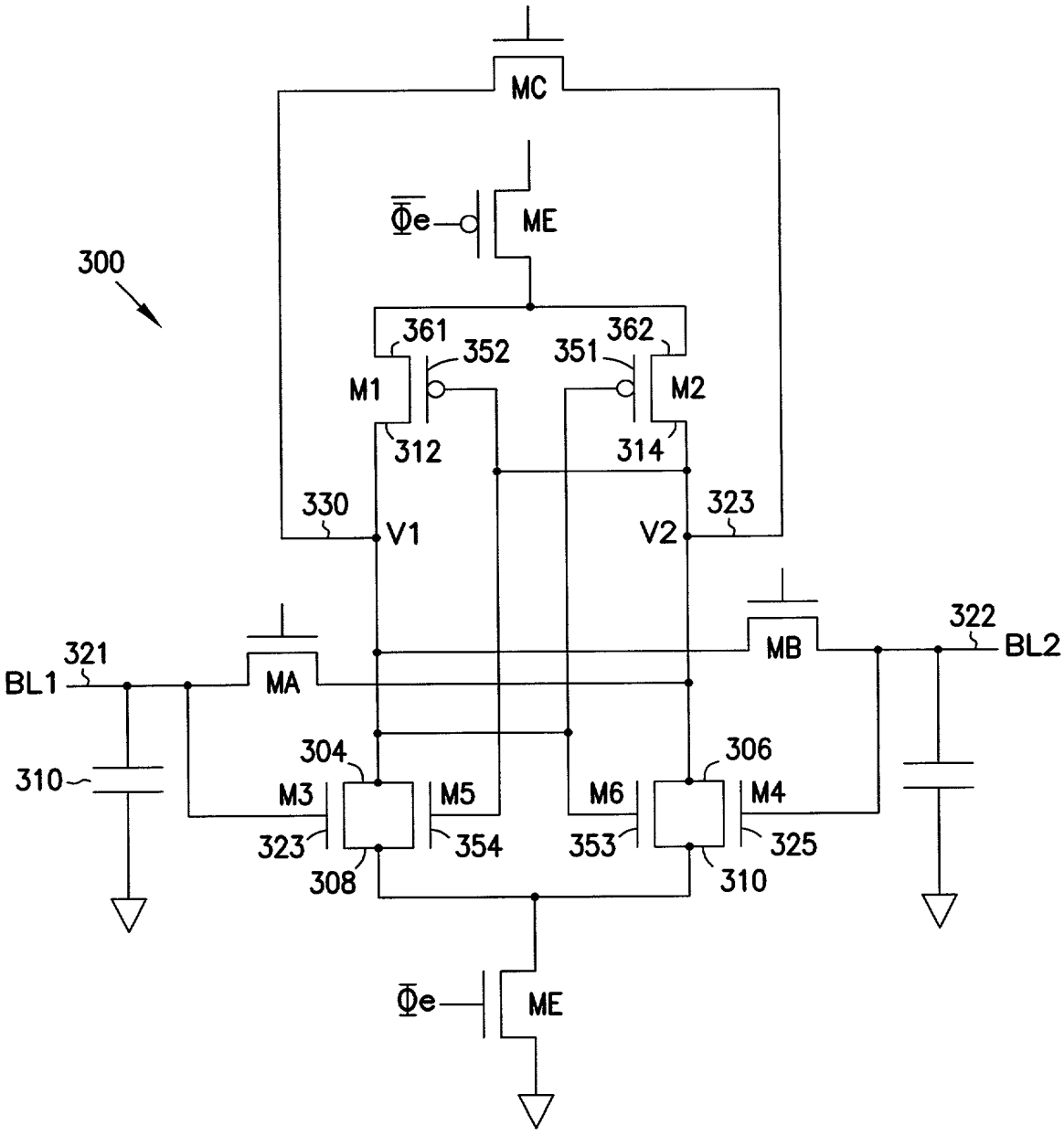
ΔV
210
CBL
ΔV
V1
I2
gmΔV/4
CS
gd
Vz
+
−
V2
232
I3
gm3Vz/4
gd
CS
+
Vx
−
I1= gm3Vx/4

FIG. 2C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ME
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361
352
351
362
M1
M2
312
314
330
V1
V2
323
322
BL2
321
BL1
MA
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304
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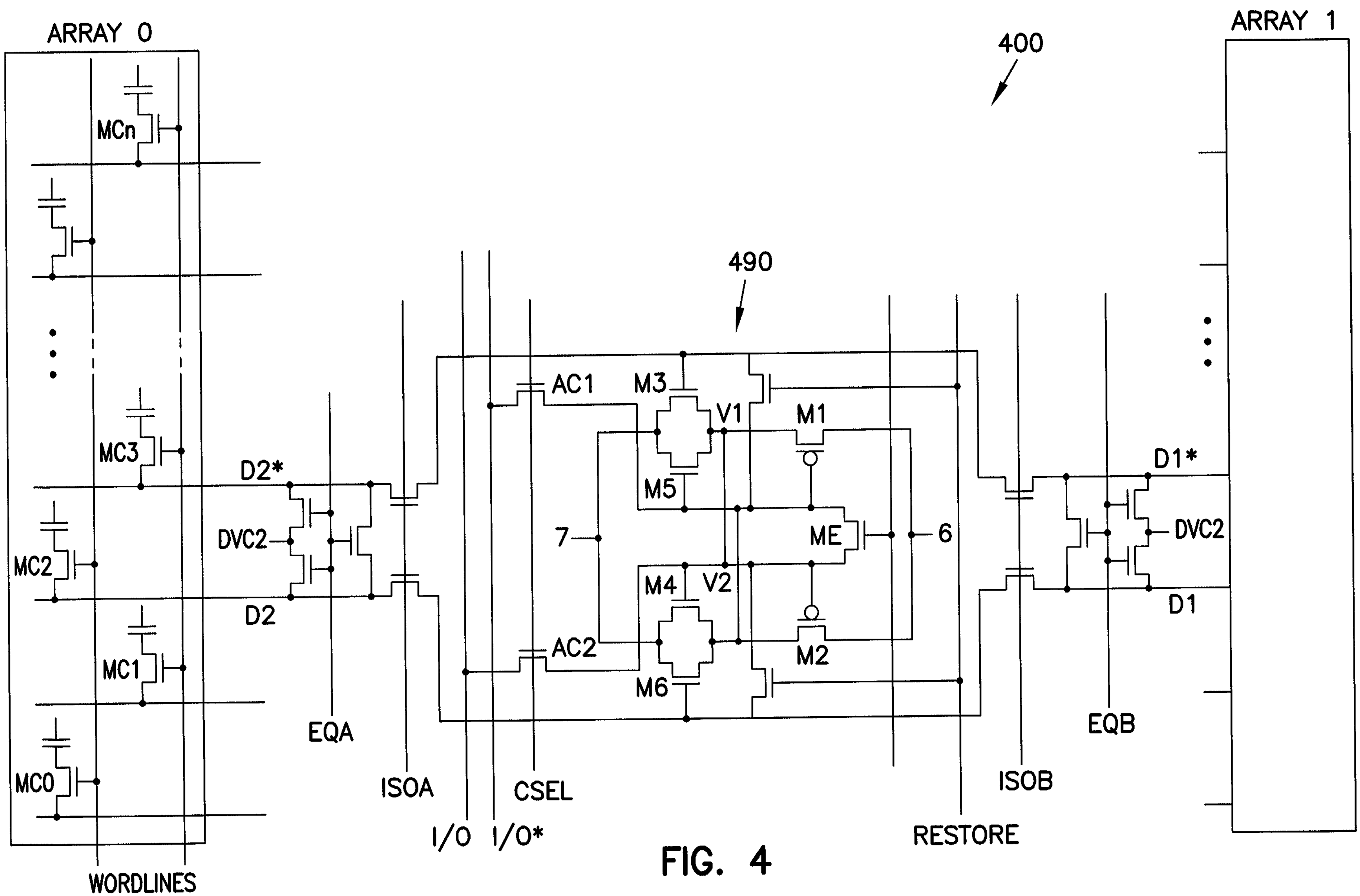
M3
M5
M6
M4
323
354
353
325
308
310
ME

FIG. 3



ARRAY 0
ARRAY 1
400
490
MCn
MC3
MC2
MC1
MC0
WORDLINES
D2*
D2
DVC2
EQA
ISOA
I/O
I/O*
CSEL
AC1
AC2
M3
M5
M4
M6
V1
V2
M1
M2
ME
7
6
RESTORE
ISOB
EQB
D1*
D1
DVC2

FIG. 4

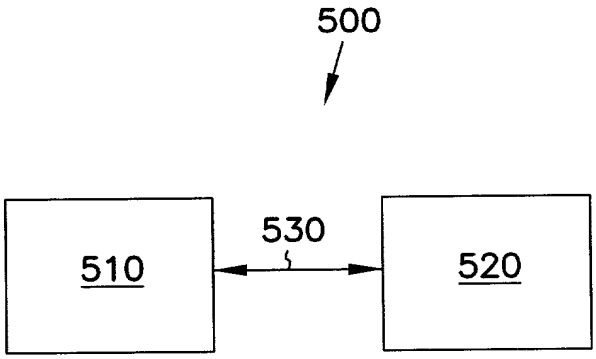


FIG. 5

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DRAM SENSE AMPLIFIER FOR LOW VOLTAGES .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: 5077 N. Fifeshire Pl.
Boise, ID 83713

Signature: Brent Keeth Date: 5/21/99
Brent Keeth

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: _____ Date: 17 MAY 99
Leonard Forbes

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Post Office Address: 5077 N. Fifeshire Pl.
Boise, ID 83713

Signature: _____ Date: _____
Brent Keeth

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.586US1	
Title:	DRAM SENSE AMPLIFIER FOR LOW VOLTAGES		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Matthew W.	Reg. No. 43,459	Fordenbacher, Paul J.	Reg. No. 42,546	Maki, Peter C.	Reg. No. 42,832
Anglin, J. Michael	Reg. No. 24,916	Forrest, Bradley A.	Reg. No. 30,837	Mates, Robert E.	Reg. No. 35,271
Arora, Suneel	Reg. No. 42,267	Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. 42,858
Bianchi, Timothy E.	Reg. No. 39,610	Holloway, Sheryl S.	Reg. No. 37,850	Nielsen, Walter W.	Reg. No. 25,539
Billion, Richard E.	Reg. No. 32,836	Huebsch, Joseph C.	Reg. No. 42,673	Oh, Allen J.	Reg. No. 42,047
Black, David W.	Reg. No. 42,331	Kalis, Janal M.	Reg. No. 37,650	Padys, Danny J.	Reg. No. 35,635
Brennan, Thomas F.	Reg. No. 35,075	Klima-Silberg, Catherine I.	Reg. No. 40,052	Polglaze, Daniel J.	Reg. No. 39,801
Brooks, Edward J., III	Reg. No. 40,925	Kluth, Daniel J.	Reg. No. 32,146	Schwegman, Micheal L.	Reg. No. 25,816
Chu, Dinh C.P.	Reg. No. P-41,676	Lacy, Rodney L.	Reg. No. 41,136	Sieffert, Kent J.	Reg. No. 41,312
Clark, Barbara J.	Reg. No. 38,107	Leffert, Thomas W.	Reg. No. 40,697	Slifer, Russell D.	Reg. No. 39,838
Drake, Eduardo E.	Reg. No. 40,594	Lemaire, Charles A.	Reg. No. 36,198	Steffey, Charles E.	Reg. No. 25,179
Eliseeva, Maria M.	Reg. No. 43,328	Litman, Mark A.	Reg. No. 26,390	Terry, Kathleen R.	Reg. No. 31,884
Embretson, Janet E.	Reg. No. 39,665	Lundberg, Steven W.	Reg. No. 30,568	Viksnins, Ann S.	Reg. No. 37,748
Fogg, David N.	Reg. No. 35,138	Mack, Lisa K.	Reg. No. 42,825	Woessner, Warren D.	Reg. No. 30,440

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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Dated: May 28, 1999

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel